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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,337	01/26/2004	Takeo Tsukamoto	NEC03P248-HSe	6964

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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 04/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,337	TSUKAMOTO, TAKEO	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 22-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 22-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tateoka et al (U.S. 4,916,087) in view of Homma et al (U.S. 2002/0068452).

As to claim 1, Tateoka discloses in figures 4a-4c a method of manufacturing a semiconductor device; which comprises: depositing, on a basic substance surface (see surface of substrate 11 as indicated in figure 1e) with a difference in level, a first film (46) through an anisotropic growth (see col. 6, lines 21-30); forming a second film (48) through an isotropic growth (see col. 6, lines 32-37).

Tateoka does not disclose a second film having a polishing rate equivalent to or less than a polishing rate of the first film to reinforce a projection formed on the first film; and polishing the first film and the second film using a ceria slurry.

Homma et al discloses in figures 2a-2b a semiconductor device, wherein a second film ("inorganic insulating film" 22) having a polishing rate equivalent to or less than a polishing rate of the first film ("organic insulating film" 23) to reinforce a projection formed on the first film (23); and polishing the first film (23) and the second film (22) using a ceria slurry (see paragraph [0017]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Tateoka by having a second

film which has a polishing rate equivalent to or less than a polishing rate of the first film to reinforce a projection formed on the first film; and polishing the first film and the second film using a ceria slurry as taught by Homma et al for controlling the pH values in the regions of the substrate (see paragraphs [0003] & [0017] in Homma et al).

As to claim 26, Tateoka discloses in figures 4a-4c a method of manufacturing a semiconductor device, anisotropically growing a first film (46) on a substance surface (a substance surface is a surface of substrate 11 as indicated in figure 1e) having differences in level (see col. 6, lines 21-30); isotropically growing a second film (48) which reinforces a projection on said first film (46) (a projection is "a part 47" of first film 46 remained on the surface of the substrate as indicated in figure 4b) (see col. 4, lines 8-17; and col. 6, lines 32-37).

Tateoka does not disclose a second film having a polishing rate that is equal to or less than a polishing rate of the first film; and polishing the first film and second film using a ceria sluny.

Homma et al discloses in figures 2a-2b a semiconductor device, wherein a second film ("inorganic insulating film" 22) having a polishing rate that is equal to or less than a polishing rate of the first film ("organic insulating film" 23); and polishing the first film (23) and second film (22) using a ceria slurry (see paragraph [0017]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Tateoka by having a second film having a polishing rate that is equal to or less than a polishing rate of the first film; and polishing the first film and second film using a ceria sluny as taught by Homma et al for controlling the pH values in the regions of the substrate (see paragraphs [0003] & [0017] in Homma et al).

As to claims 2 and 27, Tateoka discloses in figures 4a-4c a method of manufacturing a semiconductor device, wherein the difference in level comprises a trench (44).

As to claims 3 and 28, Tateoka discloses in figures 4a-4c a method of manufacturing a semiconductor device, wherein the difference in level comprises an interconnection (an interconnection between first film 46, second film 48 and the substrate 11).

As to claims 23, 24, and 25, Tateoka does not disclose polishing rate of the first film and the second film are within twenty percent of each other; or a thickness of the second film is not less than about 100 nm; or a thickness of second film is not greater than about 400 nm.

However, *polishing rate of the first film and the second film are within twenty percent of each other; or a thickness of the second film is not less than about 100 nm; or a thickness of second film is not greater than about 400 nm* would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-5 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tateoka et al (U.S. 4,916,087) in view of Homma et al (U.S. 2002/0068452) as applied to claim 1 above, and further in view of Tani et al (U.S. 6,936,478).

As to claims 4 and 29, Tateoka in view of Homma does not disclose a stopper film which is to act as a polishing stopper, having a polishing rate less than a polishing rate of the first film, is formed on an upper level section constituting the difference in level.

Tani et al (U.S. 6,936,478) discloses in figure 58 a semiconductor device, wherein a stopper film (143) which is to act as a polishing stopper, having a polishing rate less than a polishing rate of the first film ("ferroelectric film" 133), is formed on an upper level section constituting the difference in level (see figure 58, col. 4, lines 53-59). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Tateoka in view of Homma by having a stopper film which is to act as a polishing stopper, having a polishing rate less than a polishing rate of the first film, is formed on an upper level section constituting the difference in level as taught as Tani et al for functioning as stopper layer during chemical-mechanical polishing of the first film (see col. 4, lines 53-59 in Tani et al).

As to claims 5 and 30, Tateoka does not disclose the first film and second film both comprise oxide films and the stopper film comprises a nitride film. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Tateoka by using oxide material for both first and second films and a nitride material

for the stopper film for easily performing the process steps, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended used as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

5. Claims 6-7 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tateoka et al (U.S. 4,916,087) in view of Homma et al (U.S. 2002/0068452) as applied to claim 1 above, and further in view of Kanda (U.S. 6,818,539).

As to claims 6 and 7, Tateoka in view of Homma et al does not disclose the first film comprises a film formed by a high density plasma CVD (Chemical Vapor Deposition) method; and the second film comprises a film formed by one of an atmospheric CVD method, a low pressure CVD method and a plasma CVD method.

Kanda (U.S. 6,818,539) discloses in figure 1, a semiconductor device, wherein the first film (31) comprises a film formed by a high density plasma CVD (Chemical Vapor Deposition) method; and the second film (32) comprises a film formed by a plasma CVD method (see col. 7, lines 5-18). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Tateoka in view of Homma et al by using a high density plasma CVD method for forming the first film; and a plasma CVD method for forming the second film as taught by Kanda for performing the films in a prescribed period of time (see col. 7, lines 5-18 in Kanda).

As to claims 31 and 32, Tateoka discloses in figures 4a-4c a method of manufacturing a semiconductor device, comprising: anisotropically growing of the first film (46) (see col. 6, lines 21-30); and isotropically growing of second film (48) (see col. 6, lines 32-37).

Tateoka in view of Homma et al does not disclose the first film comprises a high density plasma CVD (Chemical Vapor Deposition) method; and the second film comprises forming a second film by at least one of an atmospheric CVD method, a low pressure CVD method, and a plasma CVD method.

Kanda (U.S. 6,818,539) discloses in figure 1, a semiconductor device, wherein the first film (31) comprises a high density plasma CVD (Chemical Vapor Deposition) method; and the second film (32) comprises forming a second film by a plasma CVD method (see col. 7, lines 5-18). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Tateoka in view of Homma et al by using a high density plasma CVD method for forming the first film; and a plasma CVD method for forming the second film as taught by Kanda for performing the films in a prescribed period of time (see col. 7, lines 5-18 in Kanda).

6. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tateoka et al (U.S. 4,916,087) in view of Homma et al (U.S. 2002/0068452) as applied to claim 1 above, and further in view of LIN (U.S. 2001/0050142).

Tateoka et al does not teach polishing the first and second films using ceria slurry.

Homma et al discloses in figures 2a-2b a semiconductor device, comprising: polishing the first film ("organic insulating film" 23) and second film ("inorganic insulating film" 22) using ceria slurry (see paragraph [0017]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor

device of Tateoka by polishing the first film and second film using ceria slurry as taught by Homma et al for improving the polishing of the chemical-mechanical polishing apparatus.

Tateoka et al in view of Homma et al does not teach polishing the first and second films using a slurry whose grains do not make aggregation before the polishing the first and second film.

LIN teaches in paragraph [0009] and in claims 1 & 7, a method using a slurry whose grains do not make aggregation before polishing process ("the grains of the affected slurry are prevented from being aggregated"). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Tateoka et al in view of Homma et al by using a slurry whose grains do not make aggregation before polishing process as taught by LIN for improving the polishing of the chemical-mechanical polishing apparatus (see claims 1 and 7 in LIN).

Response to Arguments

7. Applicant's arguments with respect to claims 22-32 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argued that the Tateoka et al reference fails to disclose depositing a first film through anisotropic growth.

In response, the examiner disagrees with applicant argument because Tateoka et al clearly discloses in figures 4a-4c a method having the step of: depositing a first film (46) through anisotropic growth (see col. 6, lines 21-30).

Applicant further argued that Tateoka et al reference does not teach or suggest the features of the claimed invention including depositing, on a basic substance surface with a difference in level, a first film through an anisotropic growth.

In response, the examiner disagrees with applicant argument because Tateoka et al clearly discloses in figures 4a-4c a method having the step of: depositing, on a basic substance surface with a difference in level, a first film (46) through an anisotropic growth (see col. 6, lines 21-30).

Applicant further argued that the Tateoka et al reference also does not teach or suggest the features of the claimed invention including: forming, through an isotropic growth, a second film, having a polishing rate equivalent to or less than a polishing rate of a first film and polishing the first and second films using a ceria slurry.

In response, the examiner disagrees with applicant argument because Tateoka et al clearly discloses in figures 4a-4c a method having the step of: depositing, on a basic substance surface with a difference in level, a first film (46) through an anisotropic growth (see col. 6, lines 21-30); and forming, through an isotropic growth, a second film (48) (see col. 6, lines 32-37). Tateoka et al does not disclose the step of: a second film having a polishing rate equivalent to or less than a polishing rate of a first film and polishing the first and second films using a ceria slurry. However, Homma et al (U.S. 2002/0068452) discloses in figures 2a-2b a semiconductor device, wherein a second film ("inorganic insulating film" 22) having a polishing rate equivalent to or less than a polishing rate of the first film ("organic insulating film" 23) to reinforce a projection formed on the first film (23); and polishing the first film (23) and the second film (22) using a ceria slurry (see paragraph [0017]). Therefore, it would have been obvious to a person

having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Tateoka by having a second film which has a polishing rate equivalent to or less than a polishing rate of the first film to reinforce a projection formed on the first film; and polishing the first film and the second film using a ceria slurry as taught by Homma et al for controlling the pH values in the regions of the substrate (see paragraphs [0003] & [0017] in Homma et al).

Applicant further argued that Homma et al reference clearly does not teach or suggest: depositing, on a basic substance surface with a difference in level, a first film through an anisotropic growth.

In response, the examiner agrees with applicant argument that Homma et al reference clearly does not teach or suggest: depositing, on a basic substance surface with a difference in level, a first film through an anisotropic growth. However, the primary reference of Tateoka et al already clearly disclosed in figures 4a-4c: depositing, on a basic substance surface (a basic substance surface is a surface of substrate 11 as indicated in figure 1e) with a difference in level, a first film (46) through an anisotropic growth (see col. 6, lines 21-30). Thus the secondary reference of Homma et al does not necessarily disclose the step that already disclosed in the primary reference.

Applicant further argued that one of ordinary skill in the art would not have combined the references because the references are directed to completely different matters and problems.

In response to applicant's argument, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references.

Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

Michael Trinh
Primary Examiner